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REMARKS

Initially, the applicant respectfully requests entry and consideration of the present remarks because they are believed to place the application in condition for allowance.

Claims 1 - 8 are pending. Claims 1 - 3 and 5 - 7 have been allowed. The applicant respectfully requests reconsideration and allowance of this application in view of the following remarks.

As discussed more fully below, the applicant respectfully requests that the examiner reconsider the final rejection of April 19, 2007, because the cited reference U.S. Pat. No. 6,747,946 to Kaneko *et al.* (hereafter: "Kaneko") generally fails to disclose forcing input signals of the butterfly modules located in the determining step to zero, and further fails to disclose forcing the input signals of the one or more butterfly modules of the one or more successive computational stages to zero.

Claims 4 and 8 were rejected under 35 U.S.C. 102(e) as being anticipated by Kaneko. The applicant respectfully requests that this rejection be withdrawn for the following reasons.

The examiner has asserted that Kaneko discloses a method for effectively pruning a FFT circuit by forcing the input signals (X[2] - X[4], X[6] - X[8], X[10]-X[12] and X[14] - X[8] to zero, which in turn clearly forces the input signals of successive states to zero. The examiner further asserted in response to applicant's previous arguments that it is well known that connecting a signal to ground is to force a signal to have a zero value, and that Fig. 14 of Kaneko discloses that forcing the input signal of the first stage to zero also forces the input signal of successive stages to zero.

The applicant agrees that Kaneko discloses an IFFT device in Fig. 11 in which four out of the sixteen frequency-domain input terminals are connected to ground. However, the applicant

disagrees with the examiner's assertion that because Kaneko discloses that these terminals are connected to ground, Kaneko also discloses forcing an input signal to zero. Rather, Kaneko itself discloses that ***no*** input signal is applied to these terminals. Particularly, Kaneko states:

"The other terminals among the frequency-domain terminals X[0], X[1], X[2],..., and X[15] are connected to ground, and are *not subjected to information signal pieces*." See Col. 20, Lines 4 - 7.

Therefore, because Kaneko disclose not receiving an input signal at specific terminals rather than *forcing an input signal* to zero, it is respectfully requested that the rejection of claims 4 and 8 under 35 U.S.C. 102(e) be withdrawn.

Further regarding, claim 8, as mentioned above, the examiner asserted that Fig. 14 of Kaneko discloses that forcing the input signal of the first stage to zero also forces the input signal of successive stages to zero. However, claim 8 does not merely recite that an input signal at a successive stage is zero as a result of an input signal of a previous stage being forced to zero. Rather, claim 8 recites forcing the input signals of the one or more butterfly modules *of the one or more successive computational stages* determined as needing to be pruned to zero to thereby effectively prune the one or more butterfly modules.

Assuming *arguendo* that the input terminals shown in Fig. 11 of Kaneko receiving no information signal disclose forcing an input signal to zero, Kaneko merely discloses forcing an input signal of an initial stage to zero, rather than forcing an input signal of successive computational stages to zero. Although, as shown in Fig. 14 of Kaneko, an input signal which is zero at an initial stage will also be zero at a successive stage, a signal which is already zero due to an action at a previous stage is quite different than forcing an active signal to zero, as recited in claim 8.

Therefore, because Kaneko fails to disclose forcing the input signals of the one or more butterfly modules *of the one or more successive computational stages* determined as needing to be pruned to zero to thereby effectively prune the one or more butterfly modules, it is respectfully requested that the rejection of claim 8 be withdrawn.

In view of the foregoing, the applicant submits that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,

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